**Cell Description:**This is a standard 4 input OR AND INVERT (OAI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "OAI22X1" "behavioral"

module OAI22X1 ( Y, A, B, C, D );

input A;

input C;

output Y;

input D;

input B;

assign Y = ~((A | B) & (C | D));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

(D => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| OAI22X1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI22X1 | 0.300605 | 4.006238 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI22X1 | 0.256434 | 3.278998 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI22X1 | 0.281484 | 3.527279 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI22X1 | 0.205265 | 2.716359 |

**Logic Symbol:**

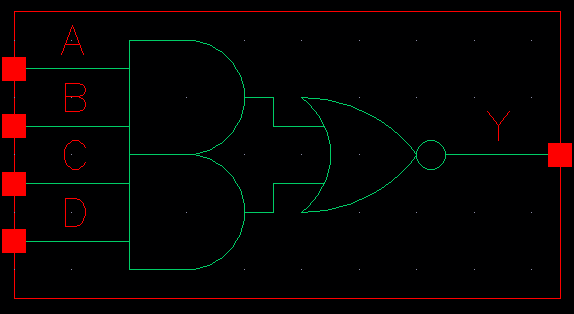
****

Figure : Symbol View for the OAI22 cell.

**CMOS Schematic:**

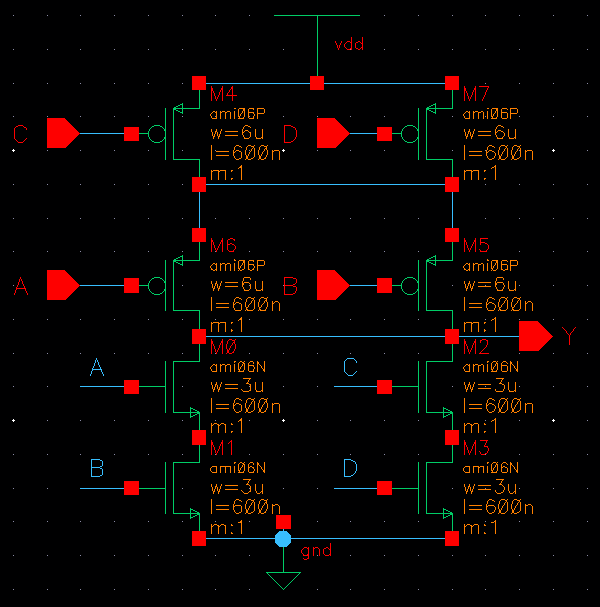
****

Figure : CMOS Schematic for the OAI22x1 cell.

**CMOS Layout:**

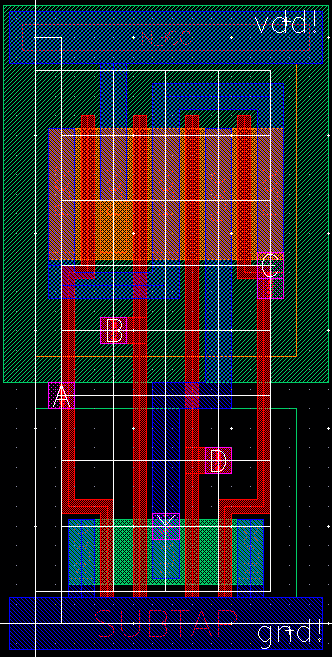
****

Figure : CMOS layout for the OAI22X1 cell.